REMARKS

Reconsideration is respectfully requested.

The presently pending Claims 1-9 have been rejected under the applicants' description of the prior art ("AAPA"), as set forth and illustrated in Fig. 2 of this application.

By this Amendment, Applicants have cancelled Claims 4 and 7, and have recited the limitations in those claims in independent Claim 1. No new matter is added.

Applicants continue to respectfully submit that the AAPA does not teach the claimed invention, as is explained in the specification pages 1-6, and in view of the arguments made below.

With respect to the indication made in the rejection of Claims 1 and 8 that the "wave-like" profile is inherently shown in the AAPA, Fig. 2, it is respectfully suggested that the "wave-like" profile cannot be formed due to complete planarization of the entire surface along the line AA', as shown in Fig. 2. Thus, the AAPA illustrated in Fig. 2 cannot but have a linear or "flat" top profile. This fact can be confirmed from the first sentence of the paragraph at page 5, line 14, *et seq.* of the specification, in which it is stated: "A general CMP process completely planarizes an entire surface regardless of the field and active areas h and t along a dotted line AA'". Accordingly, the indication in the Office Action and the Advisory Action that the AAPA describes the "wave-like" profile results from misunderstanding of the invnetion, as described and claimed, and thus, the rejection is considered improper.

The present invention is characterized in that the surface polished by CMP has the "wave-like" profile or a non-linear top profile as recited in Claim 1. The Examiner has

taken "official notice" that a CMP process of an insulating interlayer on the topology of Fig. 2 would "inherently have a wave-like profile." Applicants respectfully suggest that taking such official notice is improper because the subject matter taken in official notice is the very distinguishing feature which has been argued to provide the patentable distinction over the same prior art described by the Applicants in the AAPA. The improvement over the prior art itself, argued at pages 1-6 of the specification, is said to be "obvious" based on the *ipse dixit* of the Examiner's taking "official notice." It is respectfully suggested that this rejection is improperly based on unsupported evidence that is not found in the record of this application, and therefore a *prima facie* case of obviousness has not been set forth in the rejection. Applicants respectfully request that the best reference be cited showing the subject matter to which official notice is taken, in accordance with 37 C.F.R. § 104(c)(2). See also MPEP § 2144.03.

For the above reasons, Applicant respectfully requests reconsideration and withdrawal of the outstanding rejections. An indication of allowable subject matter is earnestly solicited.

Respectfully submitted,

January 15, 2003

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MARKED UP COPY OF CLAIM 1

1. (Twice Amended) A method of forming gates in a semiconductor device having a non-linear top profile, the method comprising the steps of:

forming a dummy gate insulating layer on a semiconductor substrate having a field oxide layer isolating the device;

depositing a dummy gate polysilicon layer and a hard mask layer on the dummy gate insulating layer sequentially;

patterning the hard mask layer into a mask pattern and patterning the dummy gate polysilicon layer and the dummy gate insulating layer using the mask pattern as an etch barrier, creating a plurality of patterned dummy gate polysilicon and insulating layers each having sidewalls, wherein the patterned dummy gate polysilicon and insulating layers are formed on the semiconductor substrate and on the field oxide layer;

forming spacers at the sidewalls of the patterned dummy gate polysilicon and insulating layers;

depositing an insulating interlayer on the resultant structure after forming the spacers;

exposing a surface of the patterned dummy gate polysilicon and insulating layers by carrying out an oxide layer chemical mechanical polishing (CMP) process utilizing a first high selection ratio sufficient to polish the insulating layer but insufficient to polish the patterned dummy gate polysilicon and insulating layers, wherein the first high selection ratio between the insulating interlayer and the dummy gate polysilicon layer is over 20;

forming a damascene structure by removing the patterned dummy gate polysilicon and insulating layers using the insulating interlayer as another etch barrier;

depositing a gate insulating layer and a gate metal layer on the entire surface of the semiconductor substrate having the damascene structure; and

exposing a surface of the insulating interlayer by carrying out a metal CMP process utilizing a second high selection ratio sufficient to polish the metal layer but insufficient to polish the insulating interlayer, wherein the second high selection ratio between the insulating interlayer and the gate metal layer is over 50.

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TO: Examiner Pham, Thanh V. Fax. No.: (703) 308-7382
Art Unit 2823

FROM: Van Economou - Ladas & Parry (312) 427-1300

DATE: January 15, 2003

RE: U. S. Patent Application No. 09/994,284

Please Deliver the attached proposed claims to Ex. Pham, Thanh V., as soon as possible. This application is under a FINAL REJECTION.

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